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Luk et. al.
YOR920030136US1
(TAD)(8728-621)

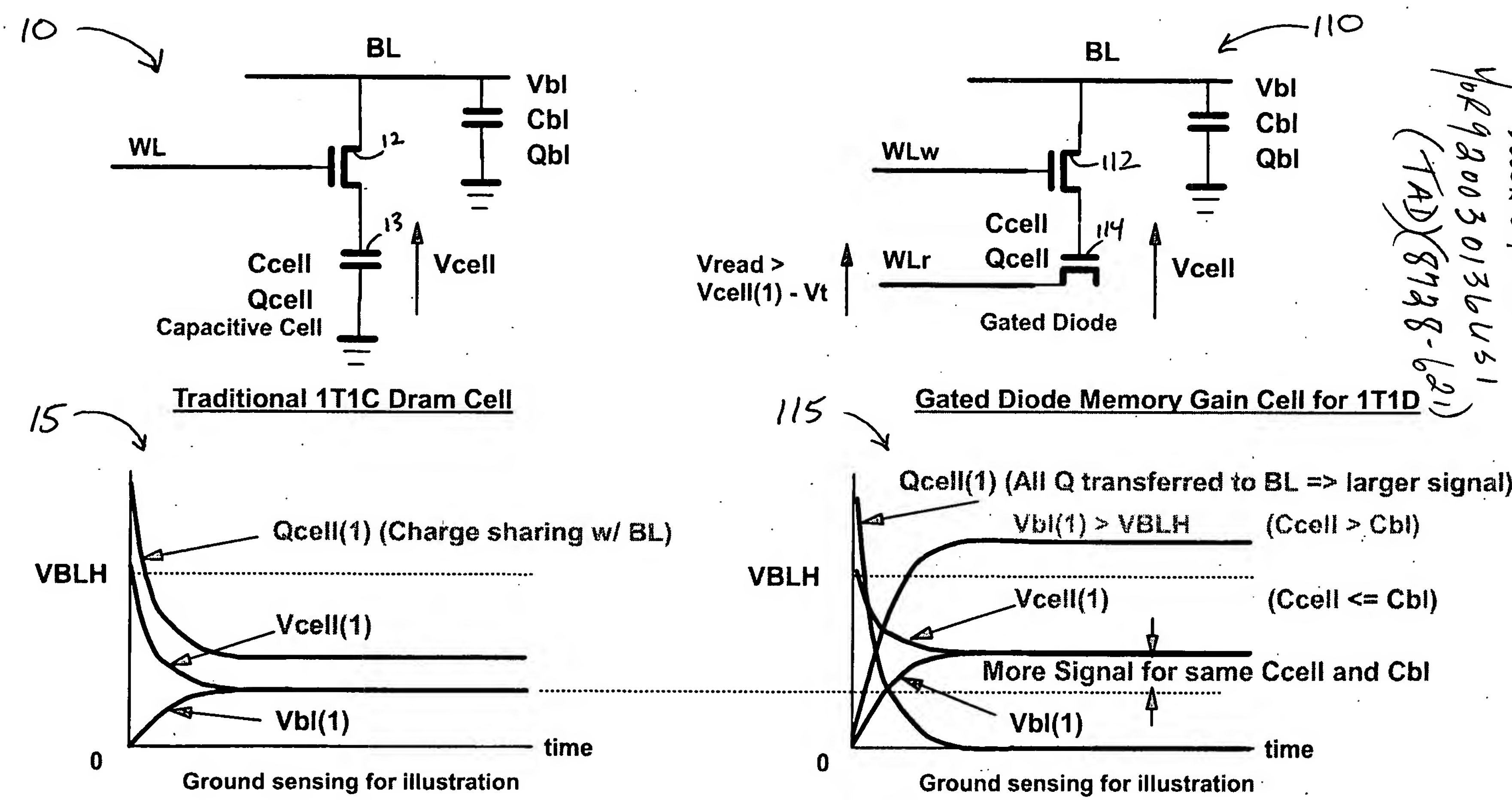


FIG. 1A

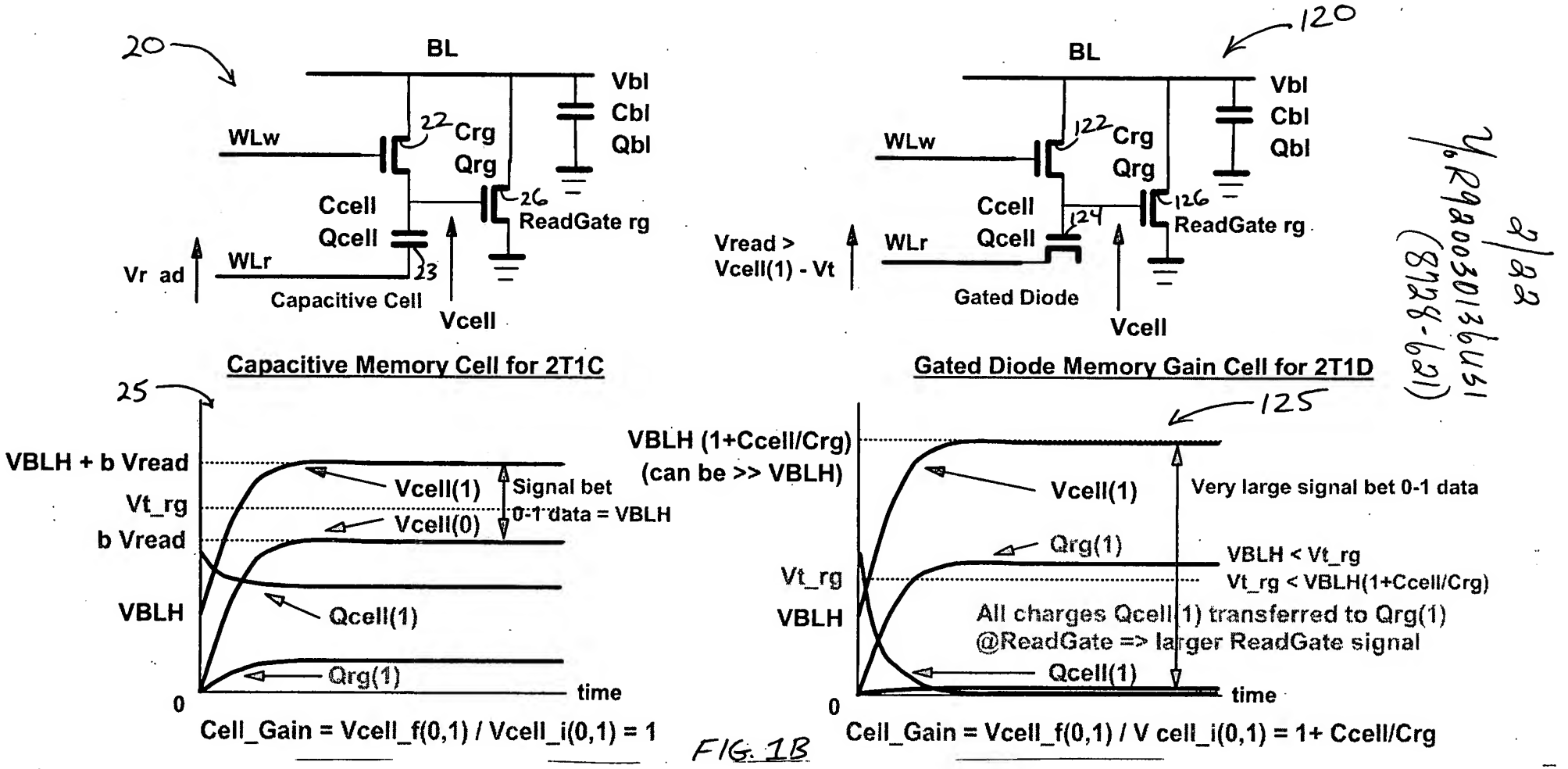
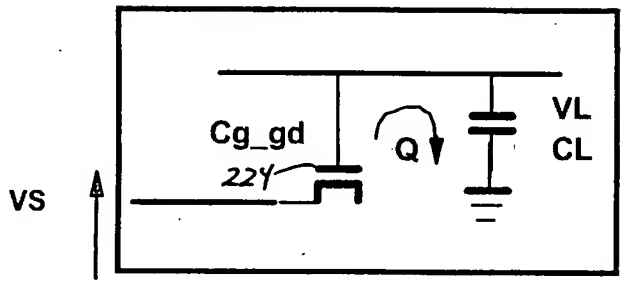
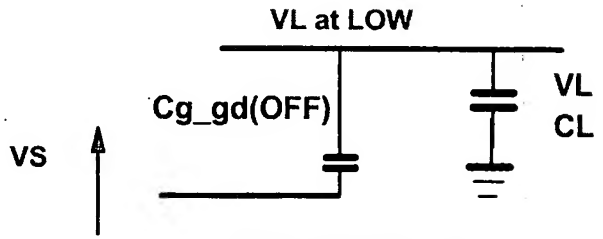


FIG. 1B

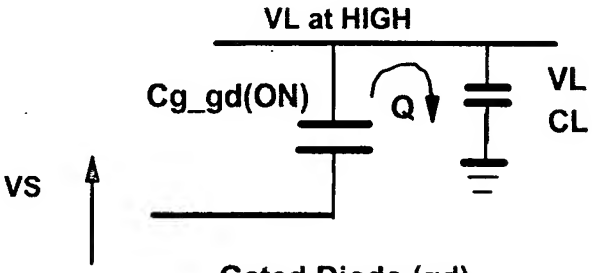
US 2003/0136951 (8928-621)



Gated Diode (gd)
Basic Structure



Gated Diode (gd)
equiv. circuit



Gated Diode (gd)
equiv. circuit

Cg_gd(ON) >> CL >> Cg_gd(OFF)
Typically, Cg_gd(OFF) : CL : Cg_gd(ON) = 1 : 10 : 100

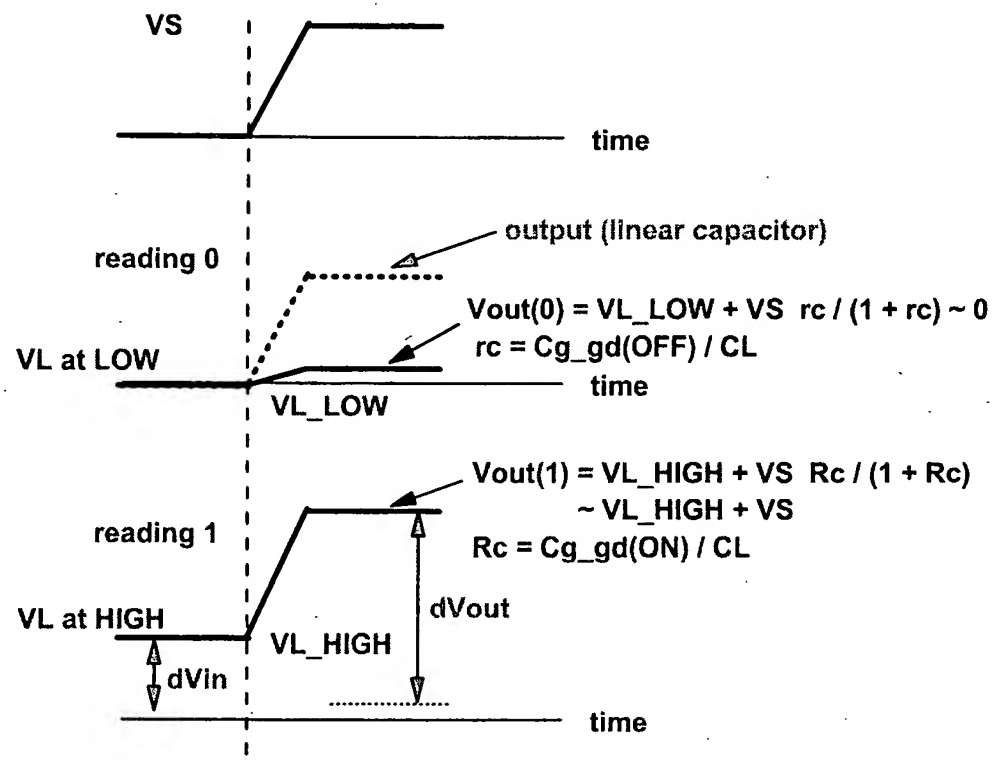


FIG. 2A

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YOR920030136US1 (8728-621)

210

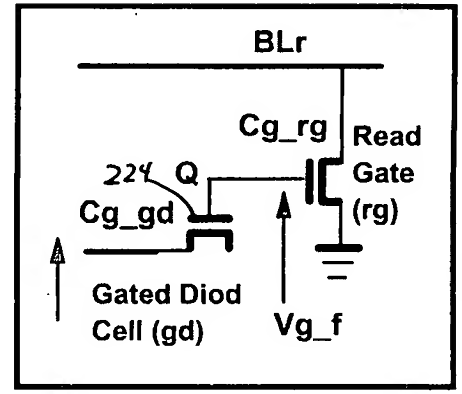
$Rc = Cg\_gd / Cg\_rg$
$Gain = Vg\_f / Vg\_i$

$Gain = 1 + Rc - (Vt\_gd / Vg\_i) Rc \sim 1 + Rc$ complete charge transfer (for small Rc)
$Gain = (1 + Vs / Vg\_i) Rc / (1 + Rc)$ constrained charge transfer (large Rc)

$Vg\_i = 0.4$ V, $Vt\_gd = 0$

typical operating point

Cg_gd / Cg_rg	0.01	0.1	1	2	5	10	100	
1 + Rc	1.01	1.1	2	3	6	11	101	
Rc / (1 + Rc)	0.01	0.09	0.5	0.67	0.83	0.91	0.99	
Gain	0.35	0.32	1.75	2.35	2.91	3.19	3.47	Vs / Vg = 2.5
Gain	0.04	0.36	2.00	2.68	3.32	3.64	3.96	Vs / Vg = 3
Charge Transfer	<---	complete	--->	<---	constrainted		--->	



@ Typical operating point
- 700 mV overdrive for Read Gate ($Vt\_rg = 0.6$ V)
- 10 - 20 x Qmin charge reserved in Gate Diode for SER protection

$Cg\_rg = 0.2$ fF, $Cg\_gd = 2+$ fF

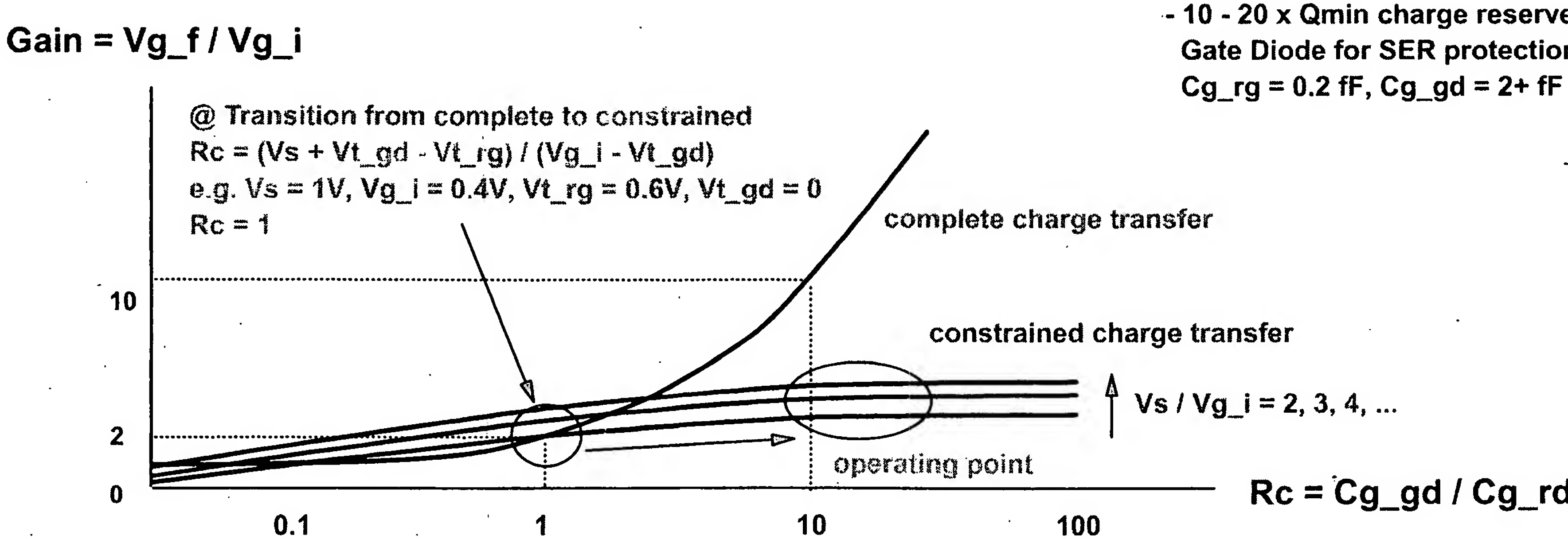
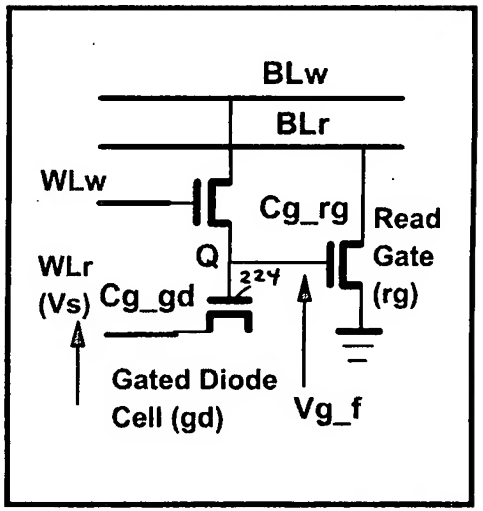


FIG. 2B



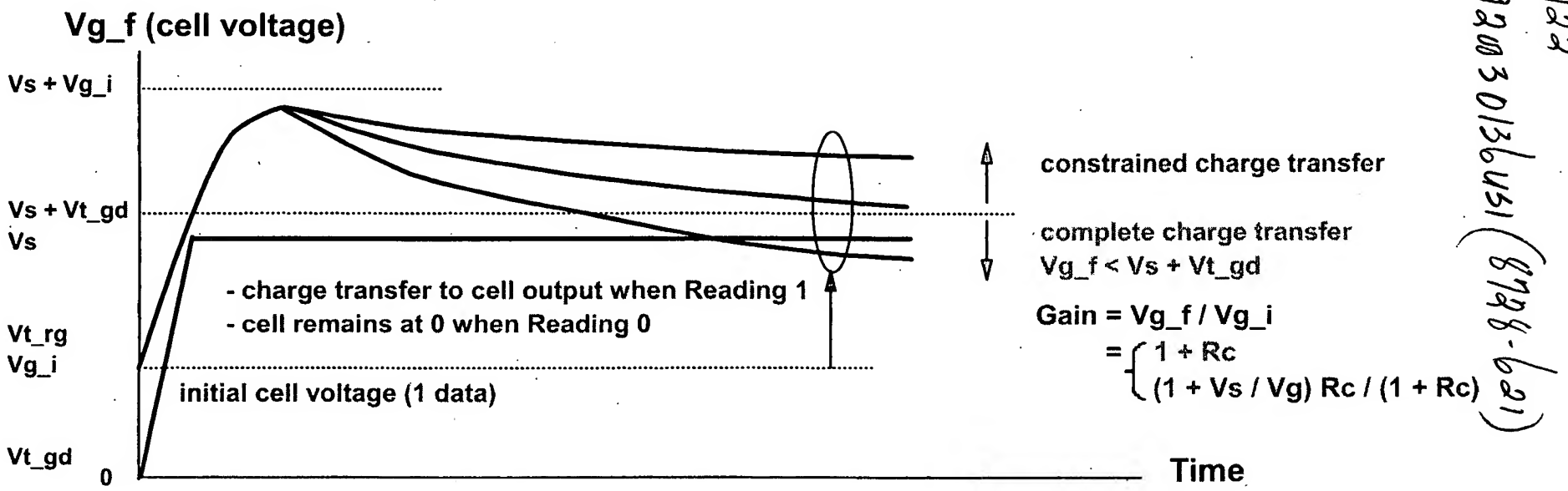
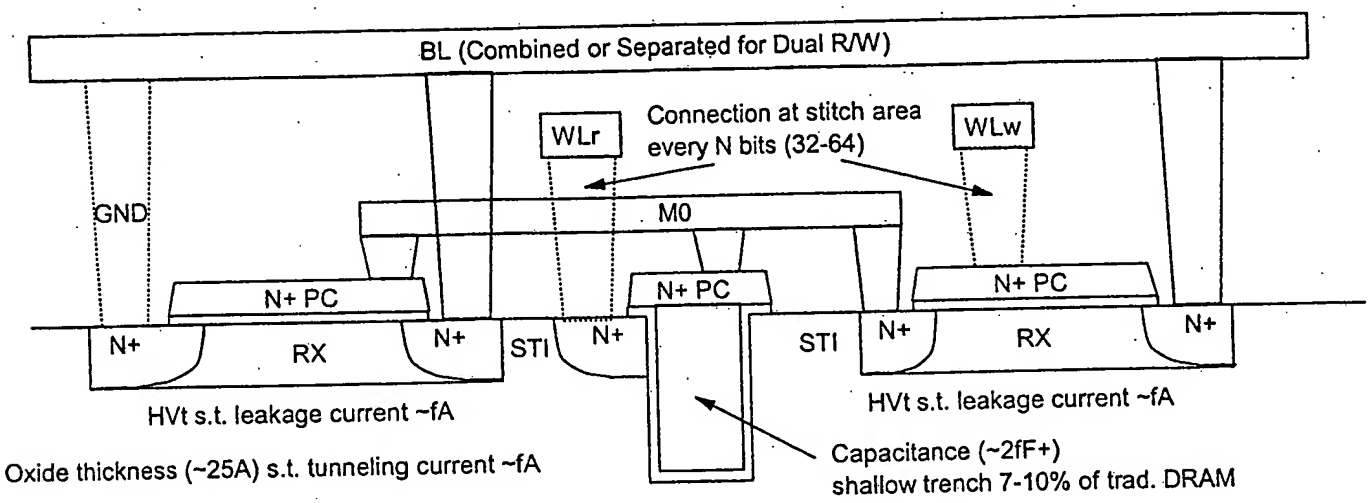


FIG. 2C

Y0R920030136US1(8728-621)

300



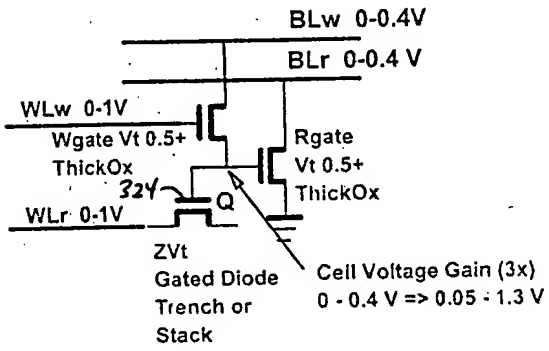


FIG. 3A

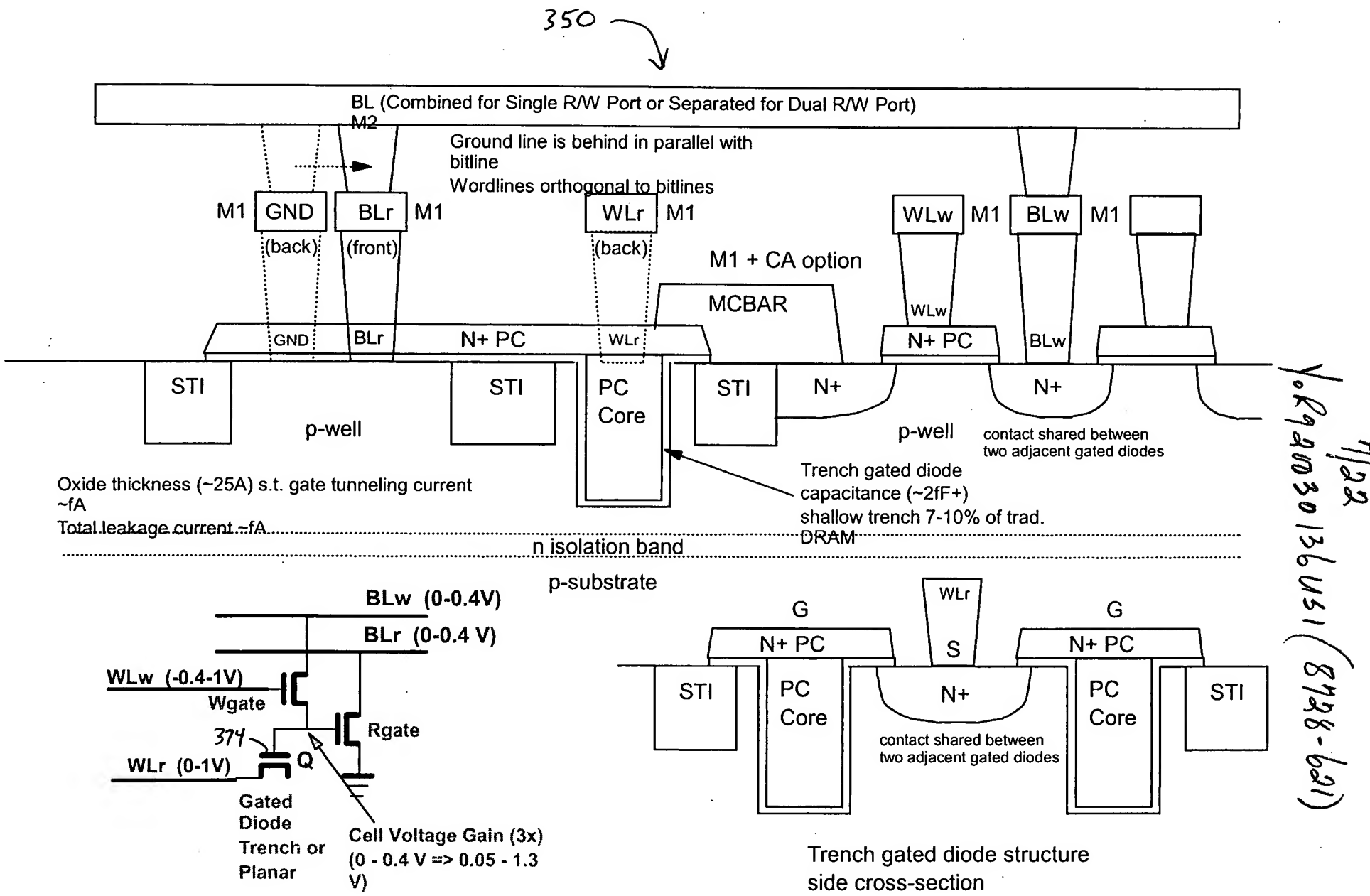


FIG. 3B

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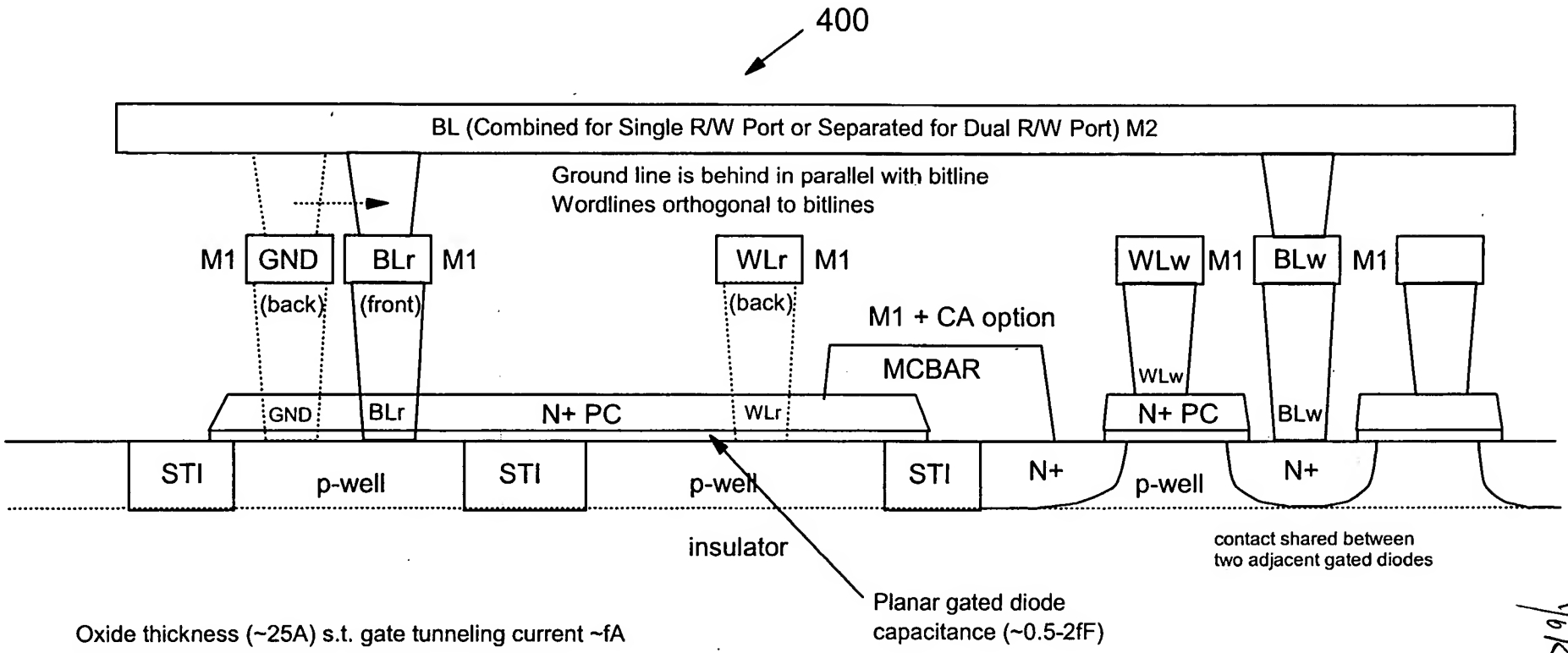
Y0R920030136US1 (8128-621)



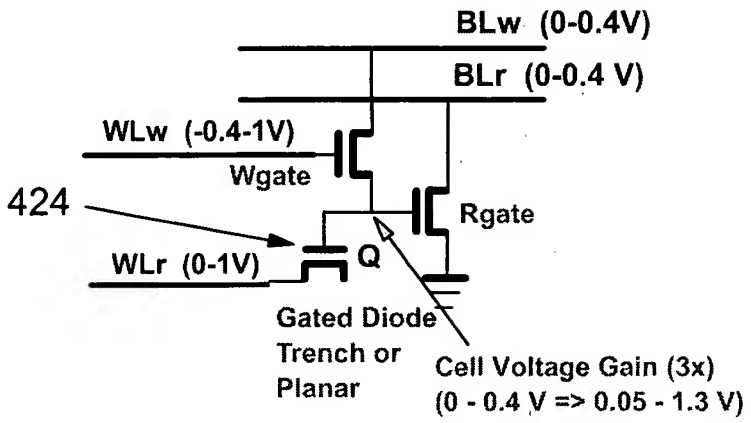


Fig. 4

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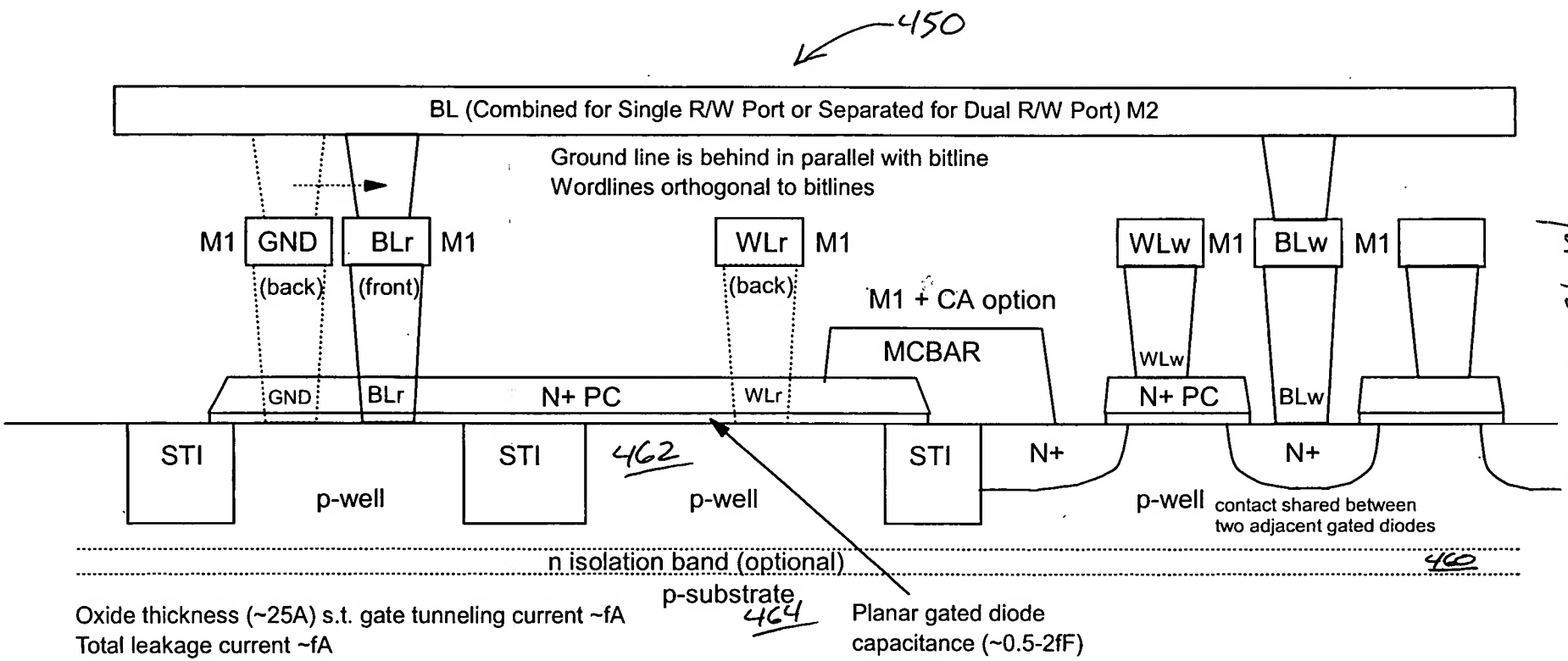

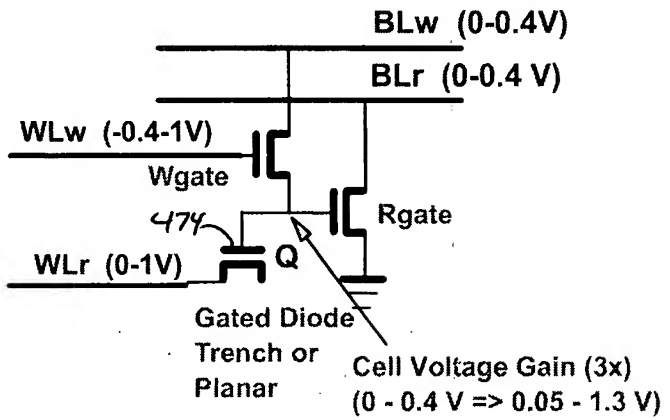

FIG. 5

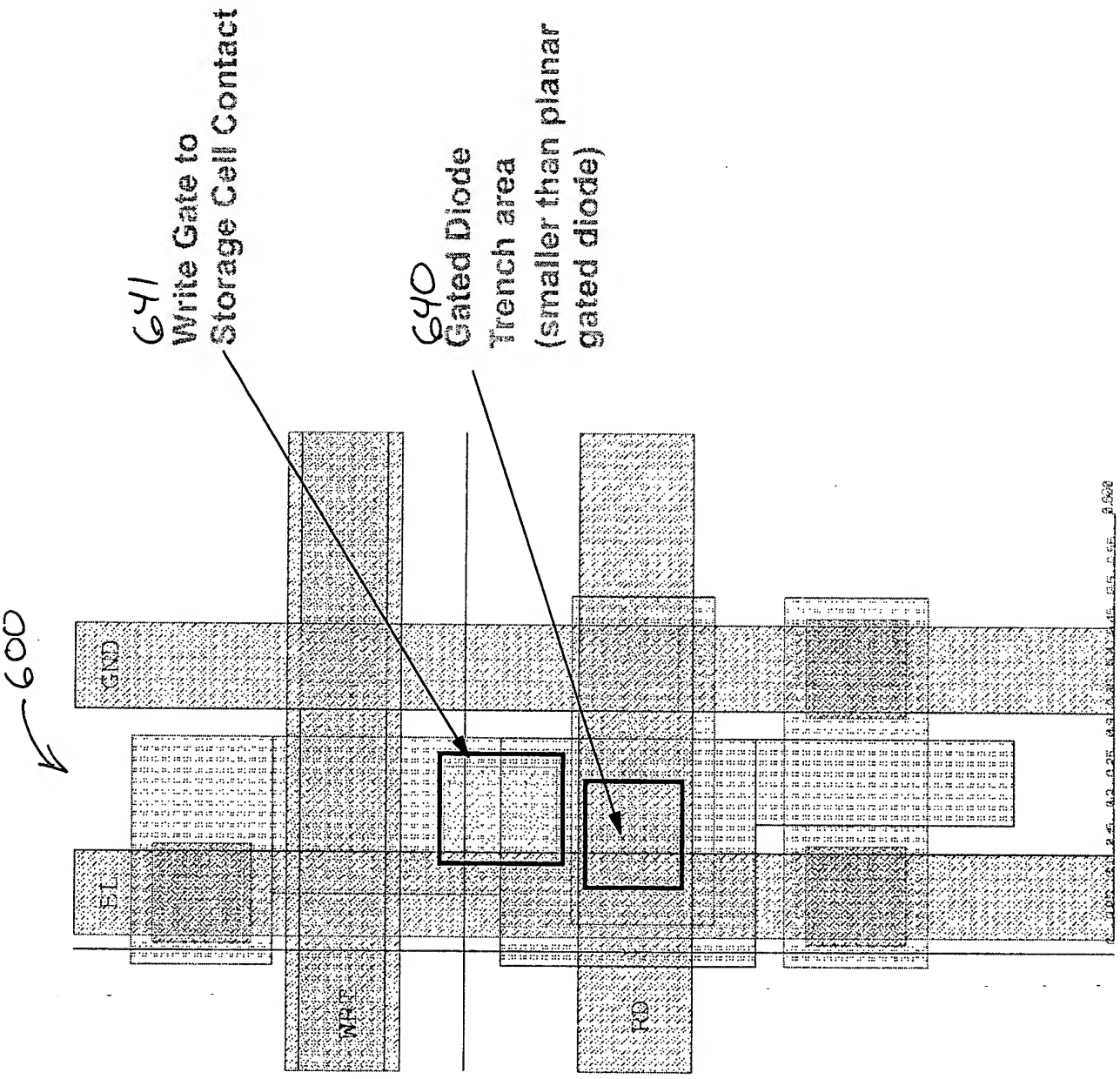
641
Write Gate to
Storage Cell Contact
640
Gated Diode
Trench area
(smaller than planar
gated diode)
600
GND
EL
WRT
FD

FIG. 6

Y0R920030136US1 (8728-621)

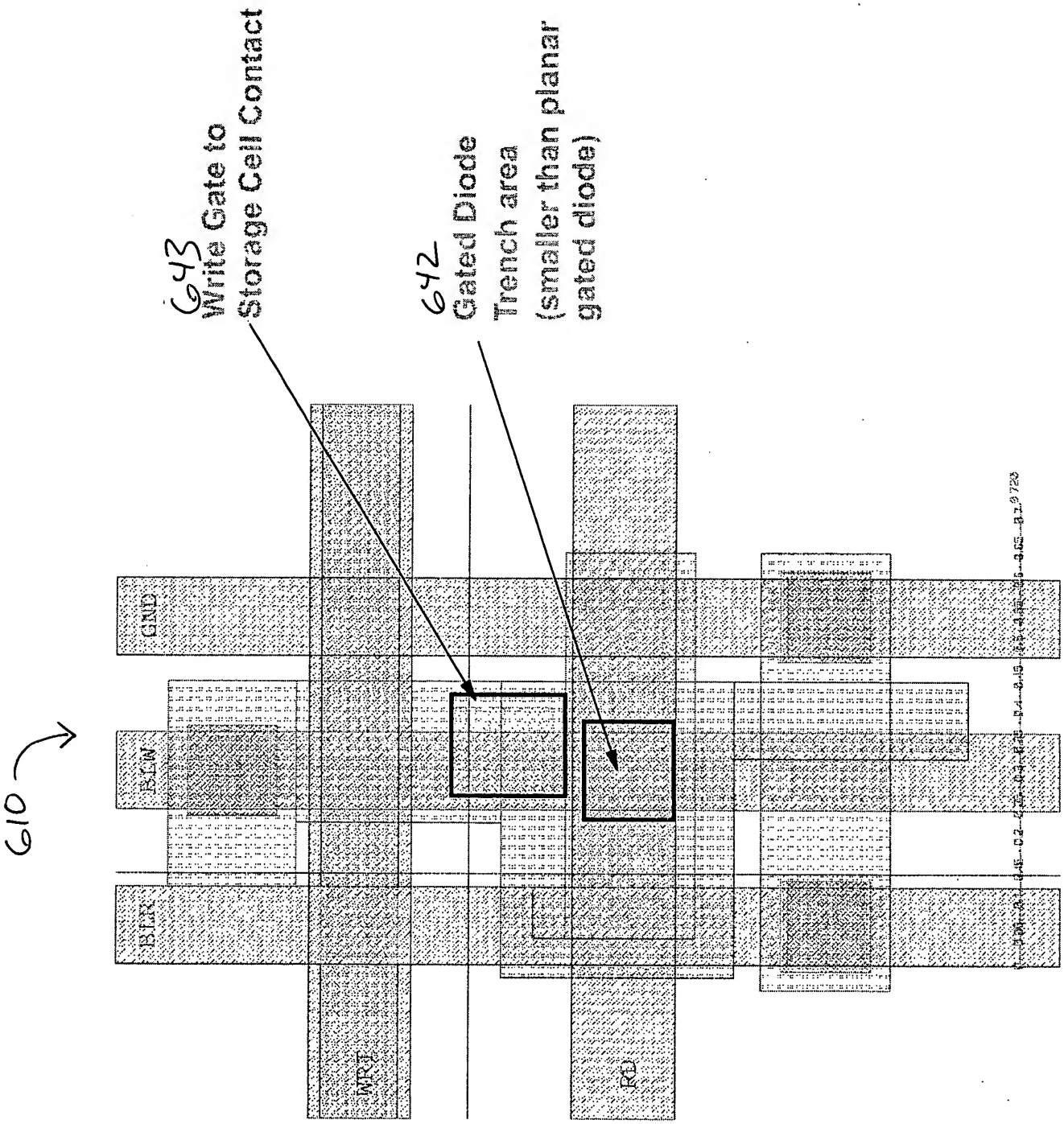

FIG. 7

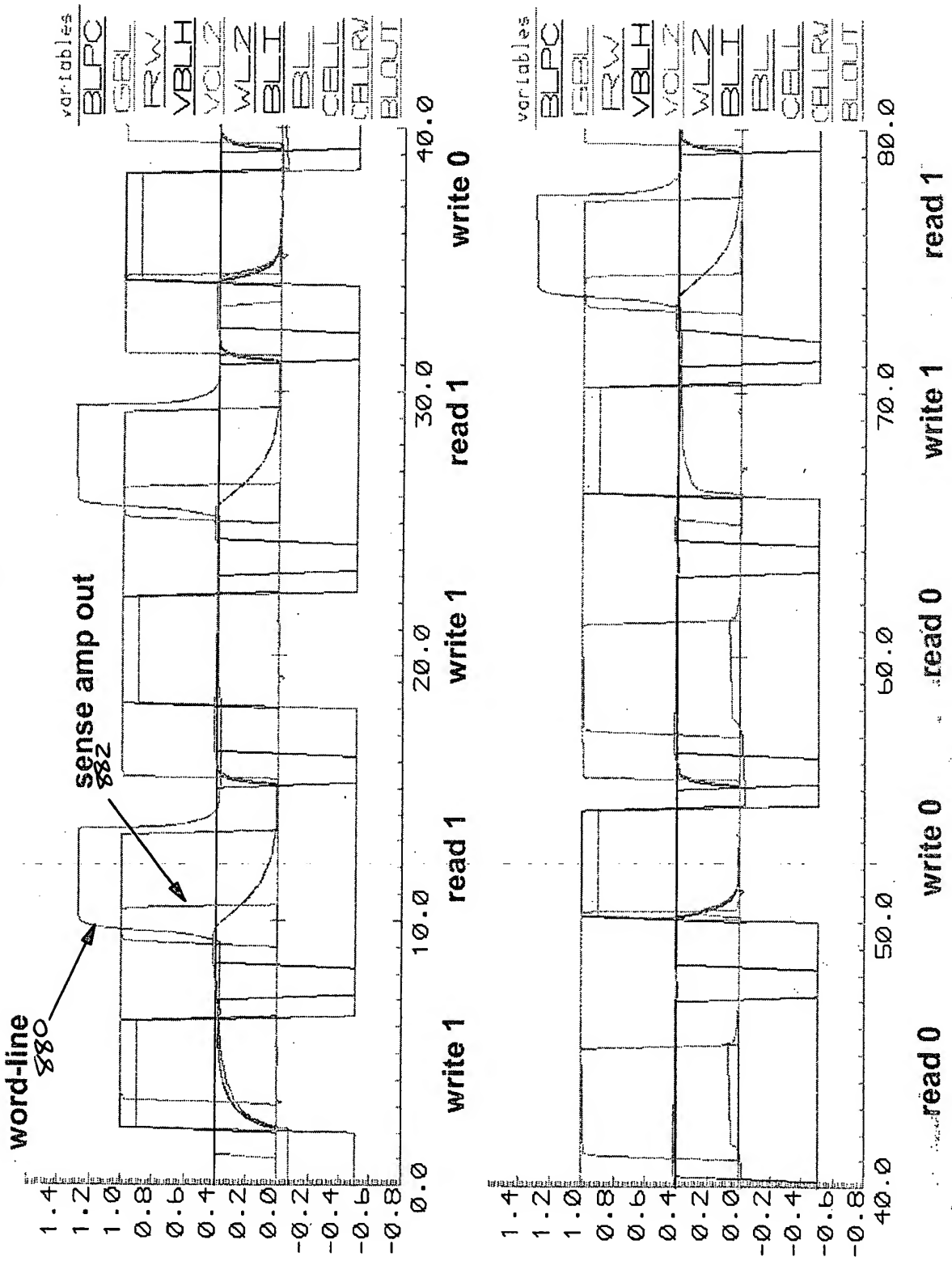
800
word-line
880
sense amp out
882
variables
BLPC
CCBL
RW
VBLH
VCLN
WLZN
BLT
BL
CELL
CELLRW
BLOUT
write 1
read 1
write 0
read 1
write 1
read 0
write 0
read 1
write 1
read 0

FIG. 8

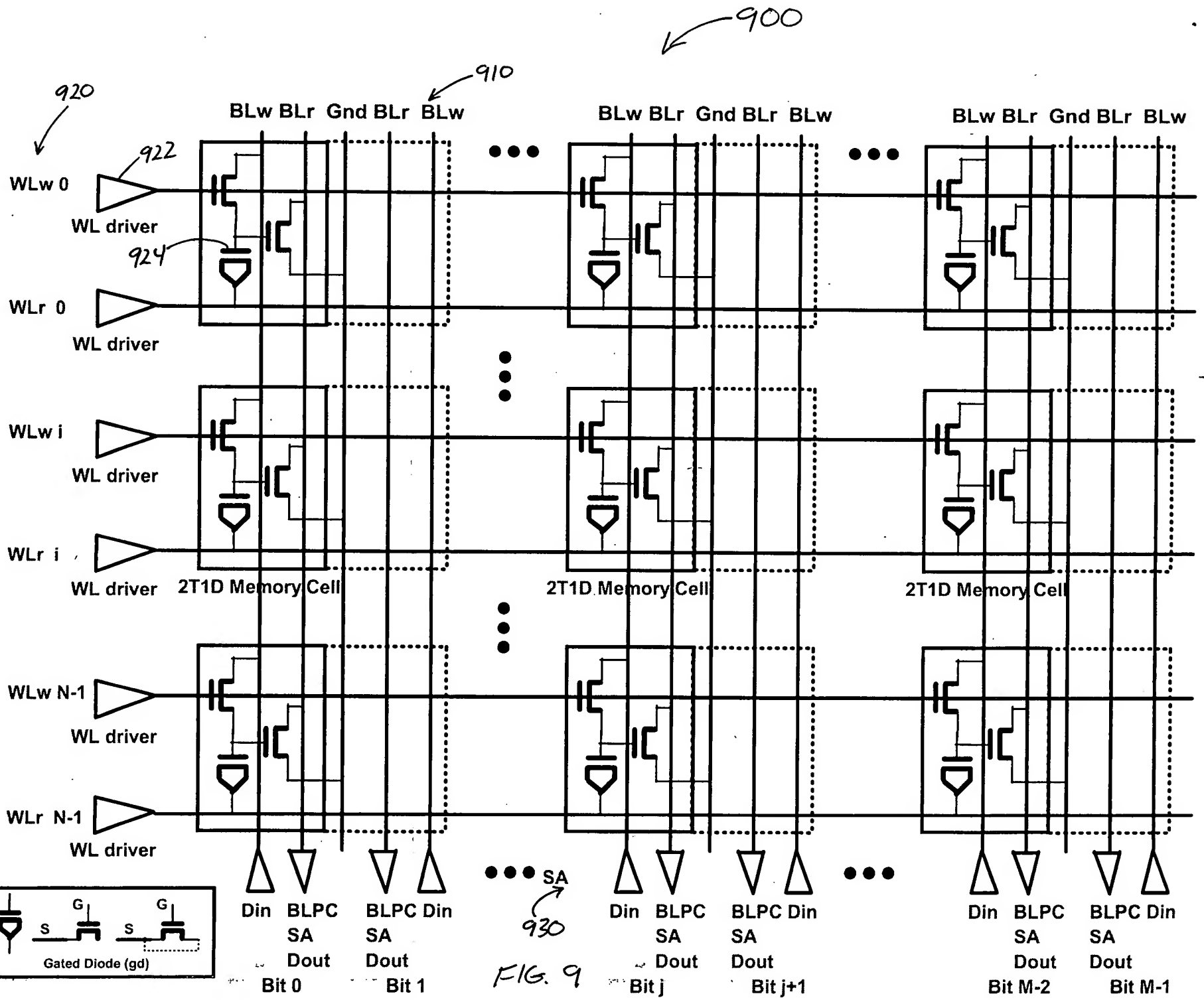
900
910
920
922
924
930
BLw BLr Gnd BLr BLw
WLw 0
WL driver
WLr 0
WL driver
WLw i
WL driver
WLr i
WL driver
2T1D Memory Cell
WLw N-1
WL driver
WLr N-1
WL driver
Din BLPC SA Dout
Bit 0
Bit 1
Bit j
Bit j+1
Bit M-2
Bit M-1
SA
G
S
Gated Diode (gd)

FIG. 9

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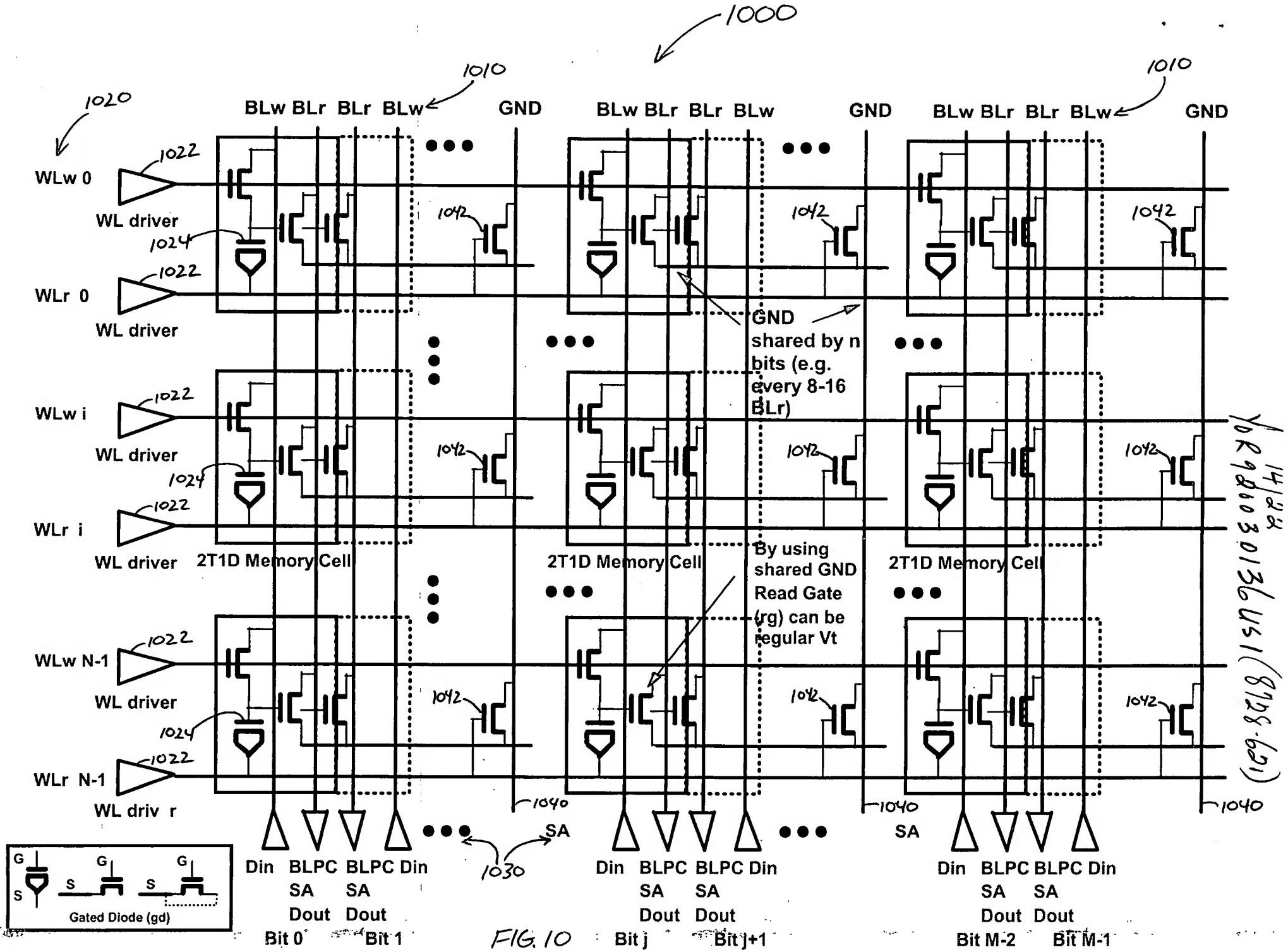

1000
1010
1020
BLw BLr BLr BLw
GND
WLw 0
WL driver
1022
1024
1042
WLr 0
WLw i
WLr i
WLw N-1
WLr N-1
WL driv r
GND shared by n bits (e.g. every 8-16 BLr)
By using shared GND Read Gate (rg) can be regular Vt
2T1D Memory Cell
1040
SA
1030
Din BLPC SA Dout BLPC SA Dout Din
Bit 0 Bit 1
Bit j Bit j+1
Bit M-2 Bit M-1
Gated Diode (gd)
G
S
FIG. 10

Figure 11A

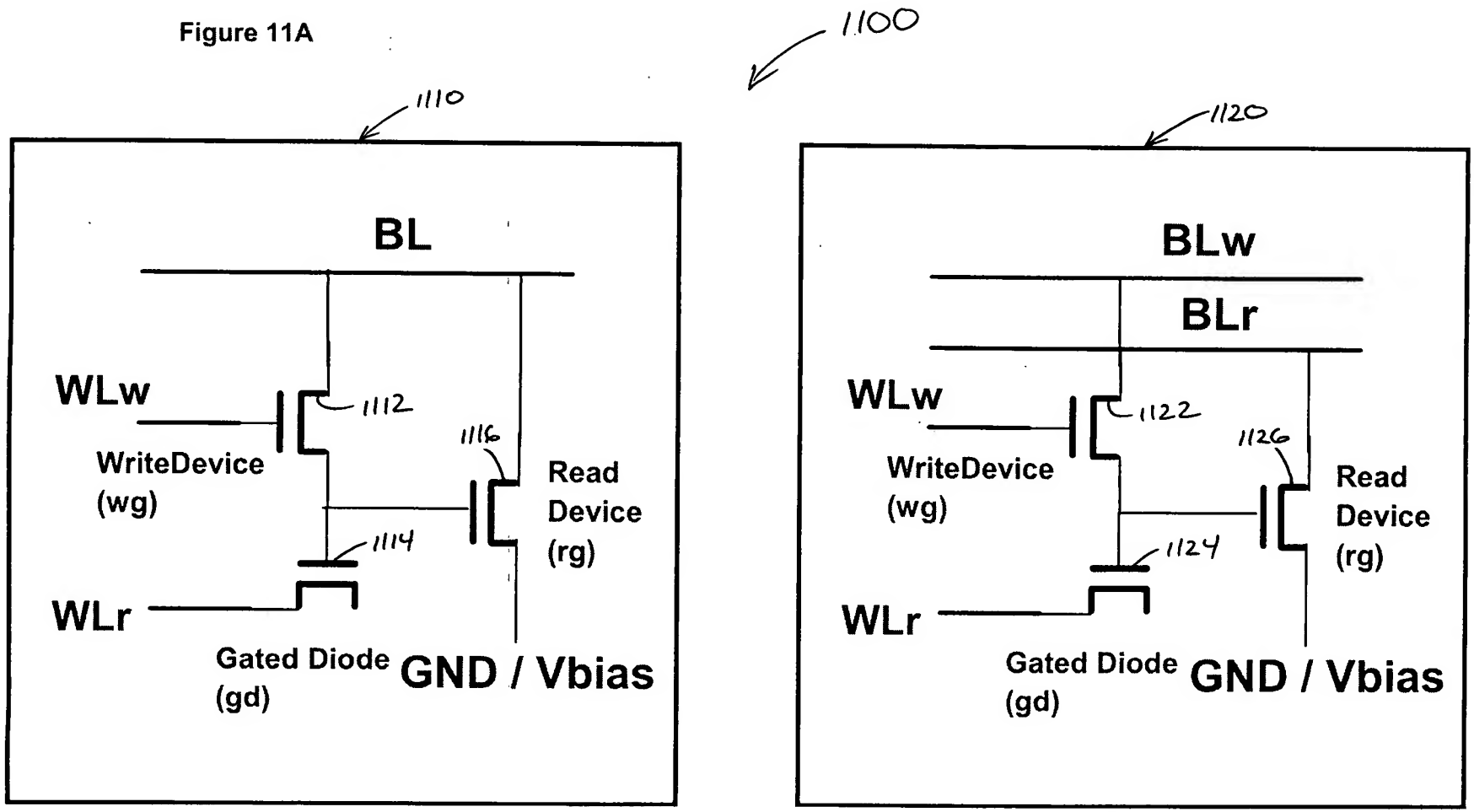
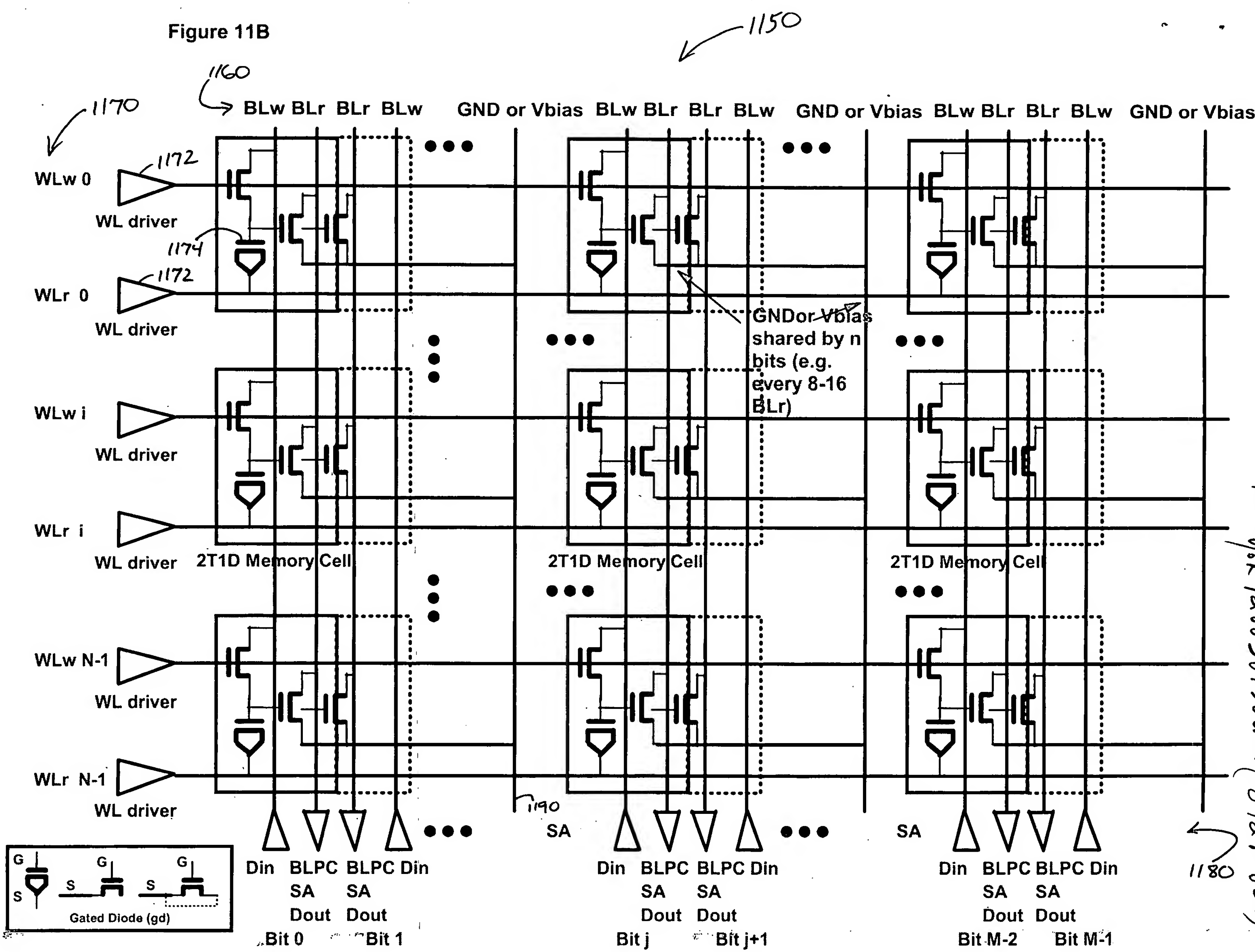


Figure 11B



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JP2003013604A1 (8728-621)

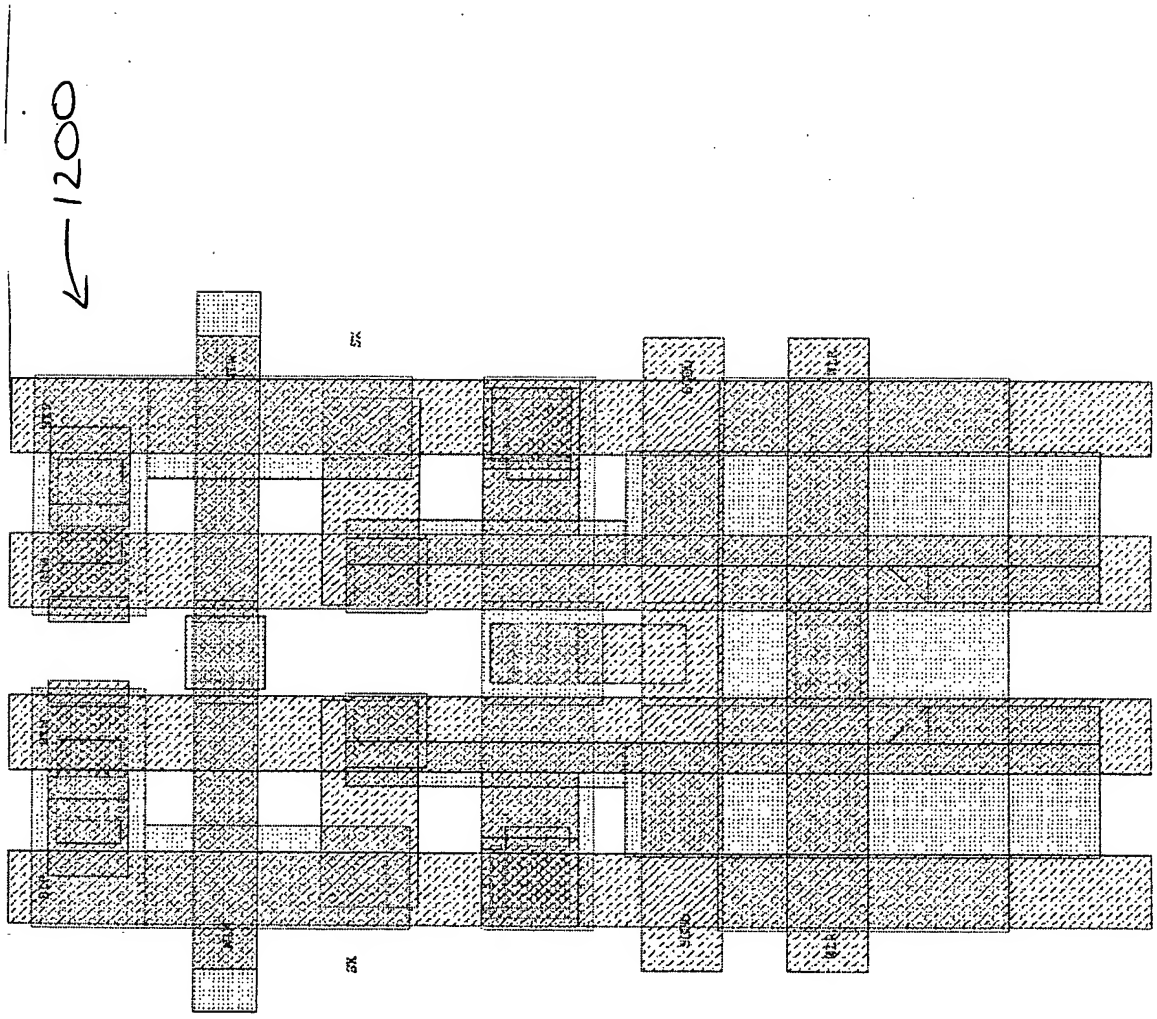

FIG. 12

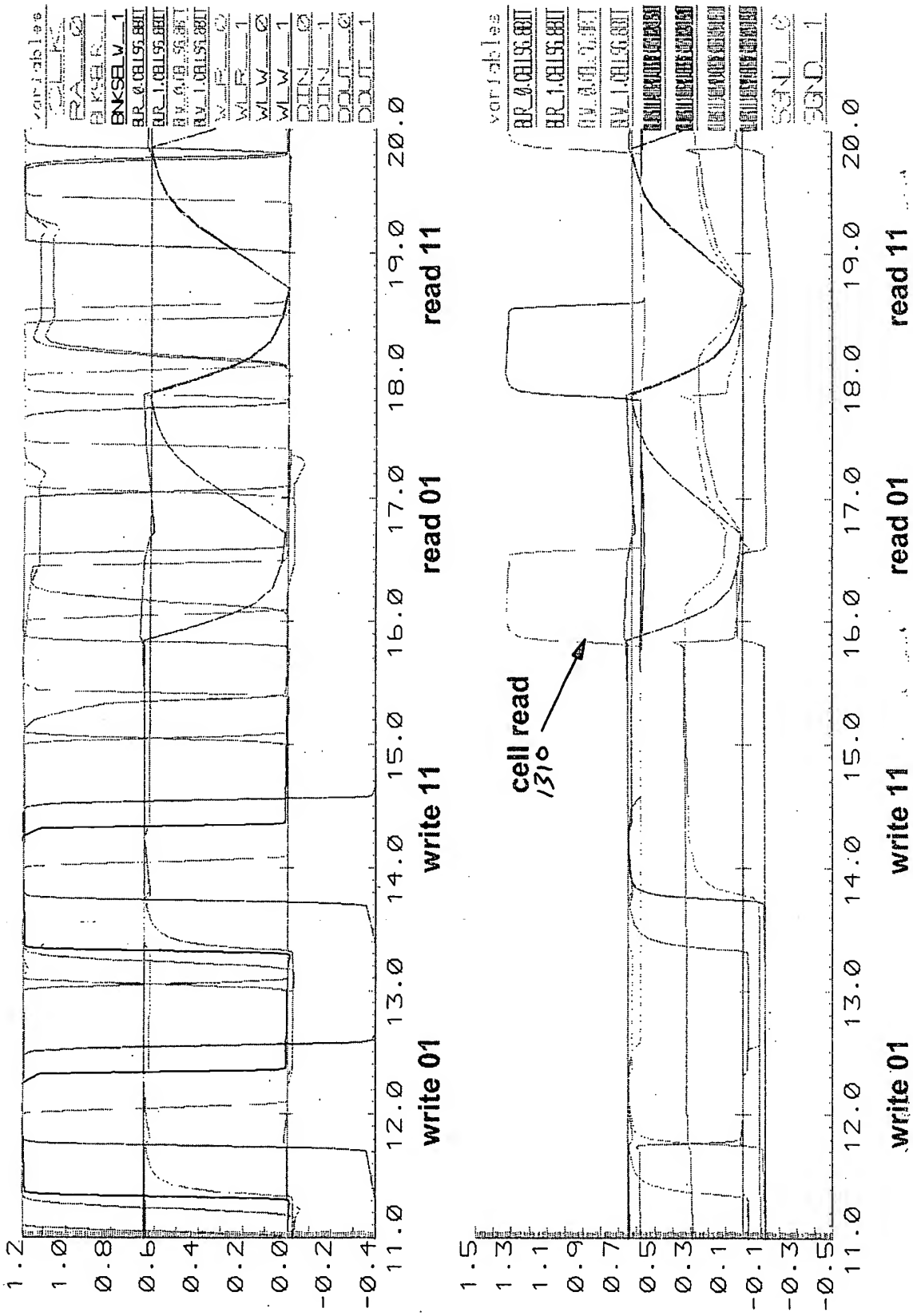
1300
write 01
write 11
read 01
read 11
cell read
1310
write 01
write 11
read 01
read 11

FIG. 13

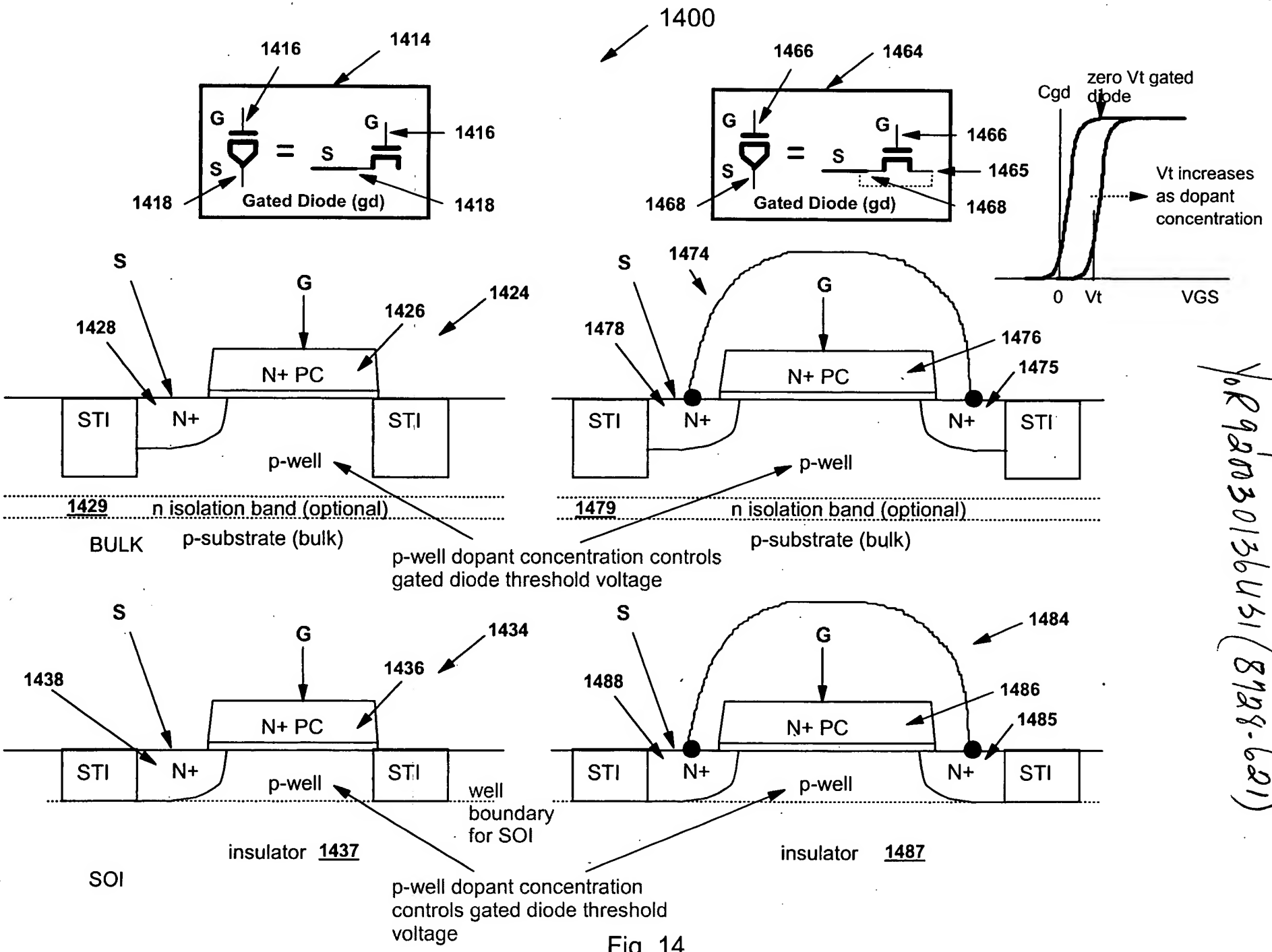

Fig. 14

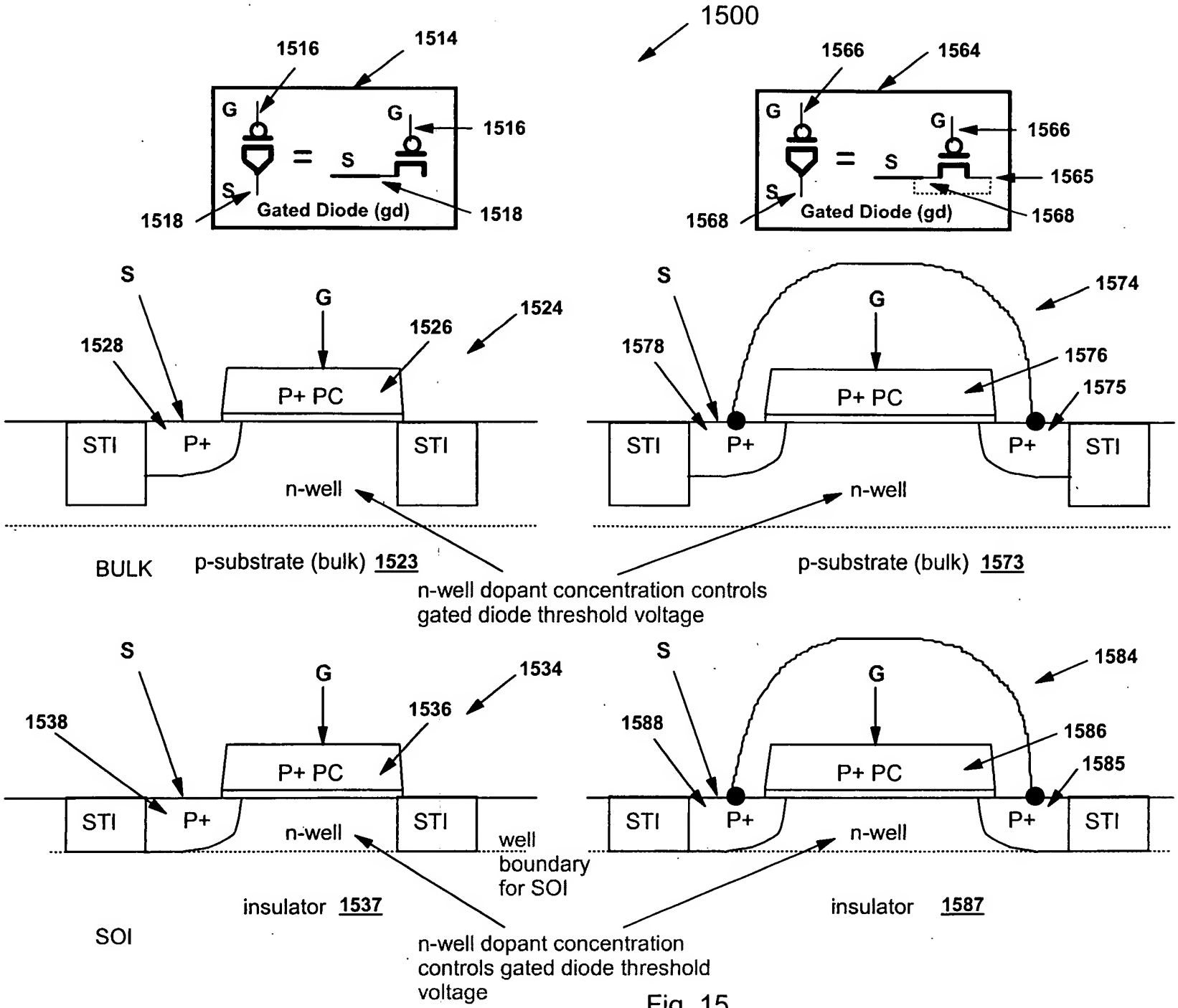

Fig. 15

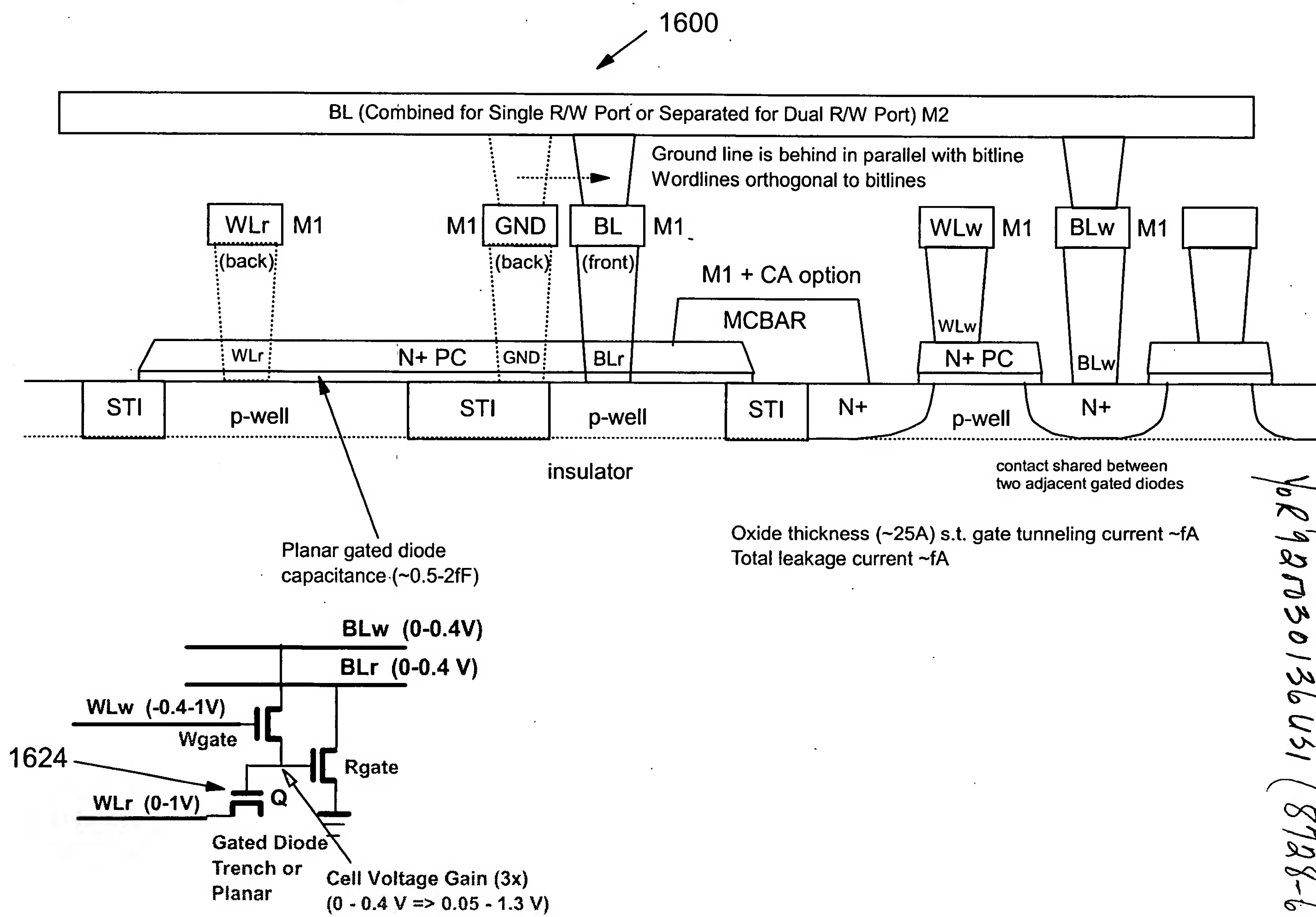
1600
BL (Combined for Single R/W Port or Separated for Dual R/W Port) M2
Ground line is behind in parallel with bitline
Wordlines orthogonal to bitlines
WLr
M1
(back)
M1
GND
(back)
BL
(front)
M1
M1 + CA option
MCBAR
WLw
M1
BLw
M1
WLr
N+ PC
GND
BLr
WLw
N+ PC
BLw
STI
p-well
STI
p-well
STI
N+
p-well
N+
insulator
contact shared between
two adjacent gated diodes
Planar gated diode
capacitance (~0.5-2fF)
Oxide thickness (~25A) s.t. gate tunneling current ~fA
Total leakage current ~fA
BLw (0-0.4V)
BLr (0-0.4 V)
WLw (-0.4-1V)
Wgate
1624
Rgate
WLr (0-1V)
Q
Gated Diode
Trench or
Planar
Cell Voltage Gain (3x)
(0 - 0.4 V => 0.05 - 1.3 V)

Fig. 16

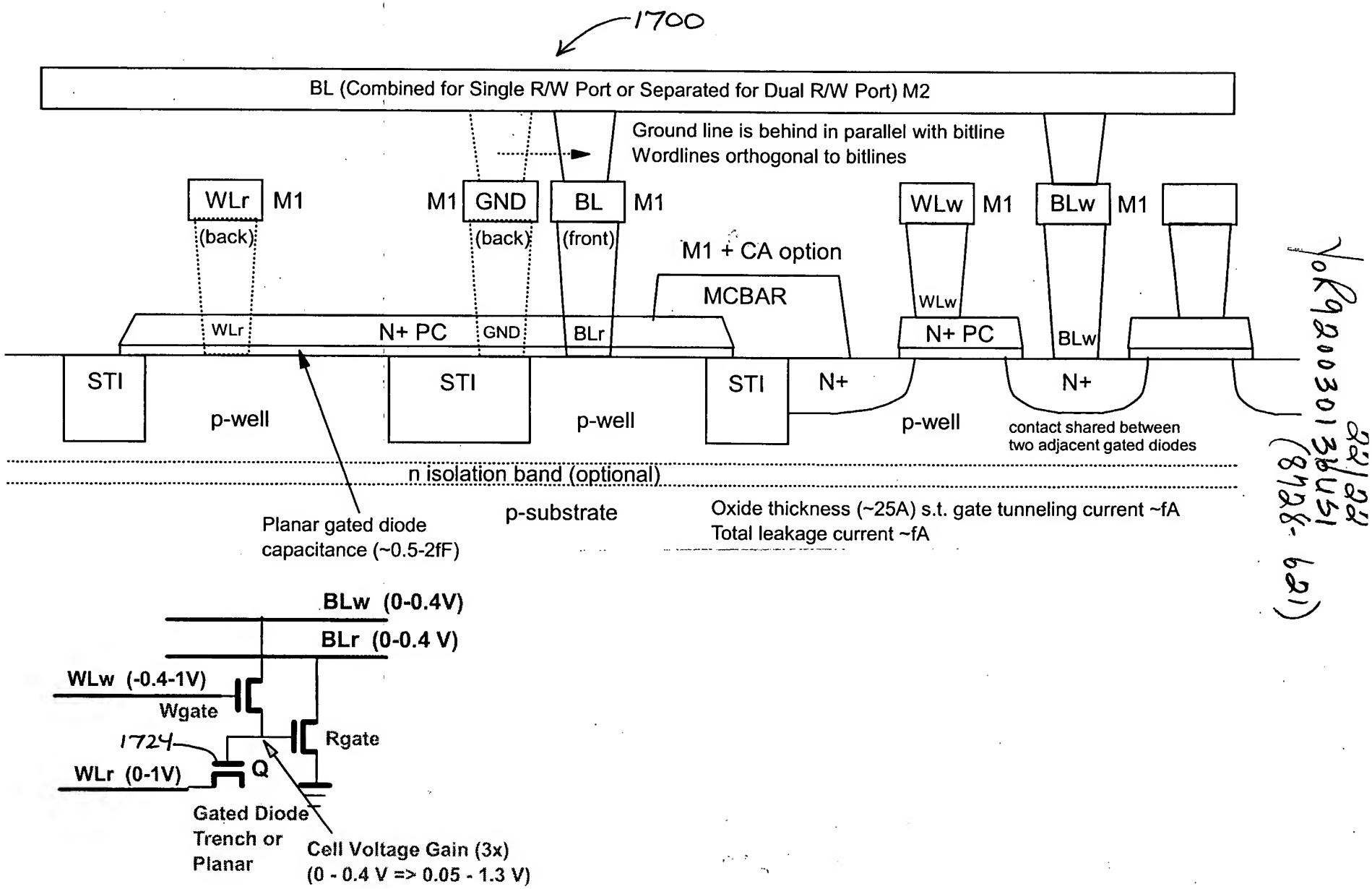
1700
BL (Combined for Single R/W Port or Separated for Dual R/W Port) M2
Ground line is behind in parallel with bitline
Wordlines orthogonal to bitlines
WLr
M1
(back)
M1
GND
(back)
BL
M1
(front)
M1 + CA option
MCBAR
WLw
M1
BLw
M1
WLr
N+ PC
GND
BLr
WLw
N+ PC
BLw
STI
STI
STI
N+
N+
p-well
p-well
p-well
contact shared between
two adjacent gated diodes
n isolation band (optional)
p-substrate
Planar gated diode
capacitance (~0.5-2fF)
Oxide thickness (~25A) s.t. gate tunneling current ~fA
Total leakage current ~fA
BLw (0-0.4V)
BLr (0-0.4 V)
WLw (-0.4-1V)
Wgate
Rgate
1724
WLr (0-1V)
Q
Gated Diode
Trench or
Planar
Cell Voltage Gain (3x)
(0 - 0.4 V => 0.05 - 1.3 V)

FIG. 17